Research on the Architecture of Lightweight PCB Defect Detection Deep Learning Model

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Abstract. In order to achieve efficient detection of printed circuit boards, this paper proposes a lightweight model for defect recognition of printed circuit boards based on the deep convolution object detection model Yolov8n. Firstly, the FasterBlock of FasterNet is introduced into the backbone network to reduce redundant calculations and memory access by means of partial convolution (PConv), which greatly improves the running speed of the network. Then, the cross-spatialmulti-scale attention mechanism (EMA)is adopted to improve the model's lightweight whilelosing some depth feature extraction capabilities. Finally, the lightweight convolution block GSConv is introduced and combined with the slim-neck structure to optimize the structure of the neck part in the original model, realizing the model lightweight and improving the computational cost effectiveness of the detector. Experimental results show that in the expanded public defect dataset PKU-Market-PCB detection, compared with the original Yolov8n, the model has the parameters reduced by 0.15%, the FPS reduced by 0.18%, and the mAP0.5 increased to 92.54%. In the future, this model can be further improved and applied to other defect detection or small target lightweight and embedded device target detection fields.

Keywords: deep learning; PCB defect detection; slim-neck structure; attention mechanism; lightweight model.

1 Introduction

With the rapid development of information technology and electronic manufacturing industry, the precision and complexity of printed circuit board (PCB) are greatly improved, which brings high difficulty in manufacturing process, which also leads to great difficulty and adjustment in defect detection. At present, in the production process of PCB, there are usually defects such as missing solder, excess copper, short circuit and so on. At present, enterprises mainly rely on automatic optical inspection technology, supplemented by manual visual inspection [1], but this detection method not only requires high cost of equipment and manpower, and its detection results are easily affected by light and imaging quality, and the detection efficiency is not high.

Yolov8, as the most advanced SOTA model from ultralytics, performs exceptionally well in both object detection and image segmentation. It builds on the previous success of YOLO and introduces new features and improvements to further improve performance and flexibility. YOLOv8n consists of three components: Backbone, Neck, and Head. The input image is first processed by the Backbone network to extract the feature map in the image. These feature maps are then fed into the Neck network, which is responsible for fusing the feature information of different levels and further passing these features to the Head prediction layer. Finally, the Head prediction layer predicts the target object and its location based on the transmitted features.

YOLOv8n can be trained on large datasets and is able to run on a variety of hardware platforms, from CPU to GPU. Therefore, Yolov8n in Yolov8 series is improved to enhance its detection ability for small target defects, improve its redundant structure in large target detection, and realize the function of PCB defect detection model that can simultaneously balance detection accuracy and detection speed. In this paper, a printed circuit board surface defect recognition algorithm FEV-YOLOv8n based on lightweight yolov8 is proposed, which adjusts the backbone network and neck network structure of the original model respectively. GSConv is used in the neck and Slim-neck structure is combined. The EMA attention mechanism was added to the backbone network and the core module in FasterNet was combined to form a new module CFE (C2f-FasterNet-EMA) to realize the lightweight design of the network.

2 Related Work

With the development of computer vision, the technology of target detection also rapidly iterates, and a series of deep network algorithms have appeared, including two-stage algorithm Faster R-CNN series [2] and one-stage algorithm YOLO series [3-5], which also provides the possibility to use deep learning methods to detect PCB board defects. At present, more and more researchers are involved in the use of deep network methods for PCB defect detection. Hu Lanlan et al [6]. proposed to use a multi-scale weighted channel network to reduce the size of the model, and finally construct a lightweight module to replace the deepest CSP structure of the backbone network, which improves the network's ability to filter redundant background information. Xu Haoxiang et al. [7] adopted the lightweight network EfficientNetLite0 as the backbone network of the model, and obtained smaller defect target features by adding P2 detection head to the feature pyramid of Yolov5 model. Li Zhongke et al. [8] improved the C2f module in Yolov8 model, combined GhostConv and DWConv to design C2F-Ghostd module to replace C2f module, and integrated PConv into Detect module, which greatly reduced the computational cost of the model and improved the accuracy to a certain extent. Liao Xinting et al. [9]introduced the SE-SiLU attention mechanism to improve the network's attention to the small defect information of shallow features by assigning weights to feature information. At the same time, a shallow feature fusion branch was added to the neck network to improve the information circulation efficiency of small defect features. Fang Qiang et al. [10]used the super-resolution generative adversarial network data enhancement method to expand the original PCB dataset, and then added the CA attention mechanism to the Yolov5 model to strengthen the model's ability to extract important feature information. Then, they designed multi-scale training instead of fixed scale training to construct a multi-scale feature fusion network. Finally, EfficientNet is used to replace the backbone network of the original model to achieve the purpose of lightweight. Li Xingchen [11] improved the three aspects of Faster RCNN respectively. Firstly, in the feature extraction network, the ResNet50 backbone network was combined with the feature pyramid to realize feature fusion. Secondly, GA-RPN was used to improve the anchor box generation method in the regional candidate network. Finally, the Pr ROI Pooling method is used in the candidate region pooling layer to avoid the candidate region error caused by quantization operation. The improved algorithm model has a good improvement in the classification, positioning and polarity direction recognition of components. Xiajun Dong [12] studied the current mainstream graphics and image recognition algorithms, and finally used the method of knowledge distillation to propose a deep learning model based on the Multi-TNet-KD method, which can be trained on embedded devices and ensure high detection accuracy. The above algorithms have greatly improved the accuracy of PCB defect detection, and the network has also been lightweight processing, but there is still a problem of large volume of model parameters, and the relationship between accuracy and speed cannot be well balanced. Therefore, there is still a large room for improvement of the lightweight design of PCB defect detection model.

3 Model Construction

3.1 Lightweight convolution module

As a new neural network proposed by CVPR in 2023, FasterNet[13] neural network runs fast on all kinds of devices and shows excellent performance in classification, detection, and segmentation tasks, while having low latency and high throughput. As its core module, FasterBlock plays a key role in the extraction of spatial features. Inside each FasterNet module, the Partial Convolution (PConv) operation is used. After PConv operation, two 1×1 ordinary convolutions are performed, and normalization and activation layers are added only after the intermediate layer to maintain the diversity of features and reduce the calculation delay.

The bottom left corner in Figure 1 illustrates how PConv works. It simply applies regular Conv on a part of the input channel for spatial feature extraction and leaves the rest of the channels unchanged. For continuous or regular memory accesses, the first or last consecutive channel is considered as a representative of the entire feature map for calculation. Without loss of generality consider the input and output feature maps to have the same number of channels.

The FLOPs of PConv is

$$FLOPs(PConv) = h \times w \times n^2 \times {c_2}^2 \quad (1)$$

In terms of computational efficiency, the FLOPs (number of floating-point operations) of PConv is only a small part of that of the regular convolution. Specifically, when the partial ratio of this part of the input channel is 1/4, the FLOPs is only 1/16 of that of the regular convolution. The amount of memory accesses is also significantly reduced, especially when the partial ratio is 1/4, which is only 1/4 of the regular convolution.

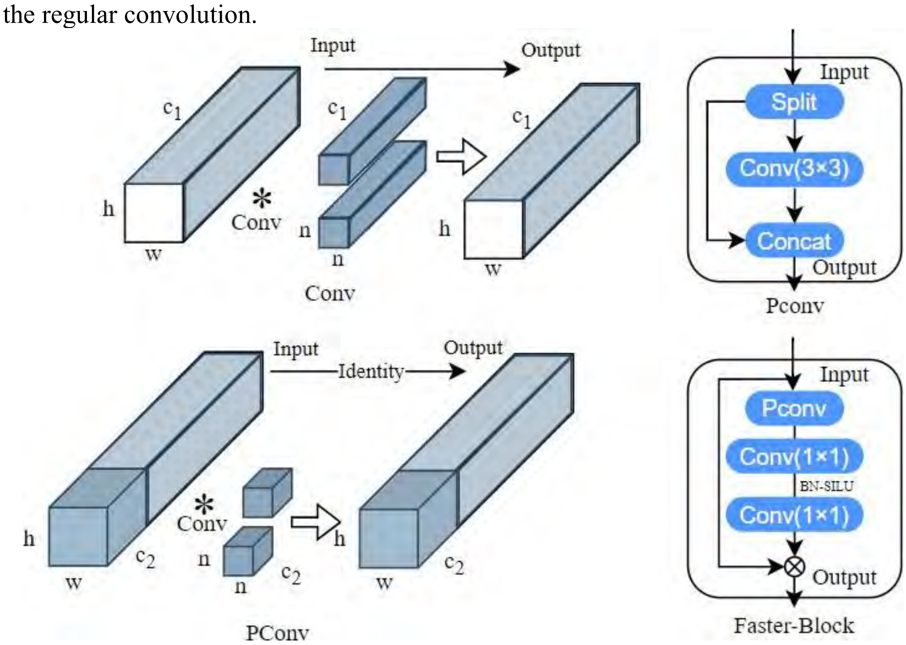

Fig. 1. Schematic diagram of Faster-Block module structure.

3.2 Introduce the attention mechanism

When the type of PCB defects is similar to the background environment, it may cause the detection model to confuse the interference information in the picture with the feature information of the target, affecting the accuracy of recognition, and causing missed detection and false detection. In order to solve the interference problem of background environment on the feature extraction of the image to be detected, the attention mechanism is usually introduced to adjust the weight allocation of the model to each area in the image, enhance the attention of the model to the target area, and improve the detection model's ability to extract defect features under complex backgrounds.

When using channel or spatial attention mechanism, the significant effectiveness in generating clearer feature representation has been proved. However, modeling cross-channel relationships through channel dimensionality reduction may have side effects on extracting deep visual representations. In order to preserve the information on each channel and reduce the computational overhead, the Multi-scale Attention (EMA[14]) module is introduced to reshape part of the channels into batch dimensions, and the channel dimensions are grouped into multiple sub-features, so that the spatial semantic features are evenly distributed in each feature group.

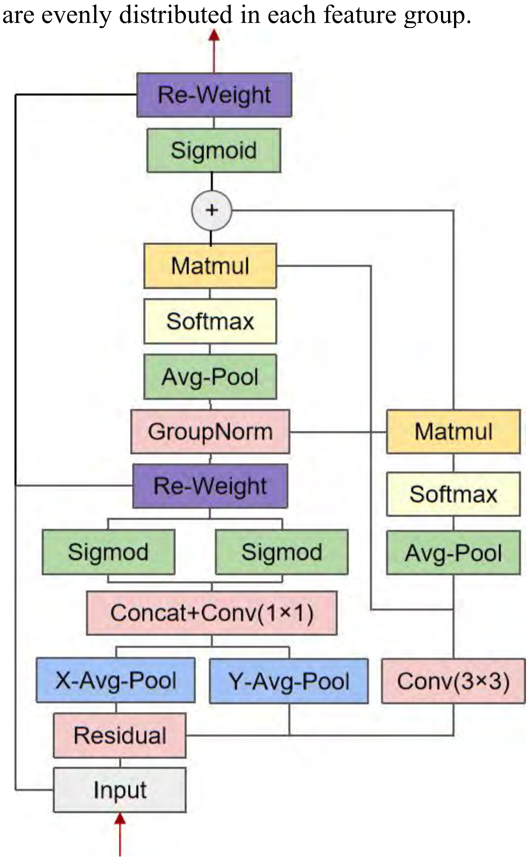

Fig. 2. EMA structure diagram.

The structure of the attention mechanism of EMA is shown in Figure 2. The core of the attention mechanism is that it combines the cross-scale space learning mechanism, which can effectively extract and amplify the feature information that is crucial to the final classification or detection results without increasing too much computational burden. This feature makes it an ideal choice for many computer vision tasks. Specifically, two pathways in EMA use a 1x1 convolutional branch, while the third takes a 3x3 branch. The 1x1 convolutional branch is mainly used to model cross-channel information interaction in the channel direction, while the 3x3 convolutional branch is able to capture broader spatial context information. Through this parallel structure, EMA is able to simultaneously manage computational resources and effectively implement dependency modeling in all channels. This parallel substructure of EMA helps the network to avoid excessive sequential processing and deep hierarchical structure, thus improving the overall processing efficiency. In addition, EMA also provides cross-spatial information aggregation in different spatial dimension directions, which helps to achieve richer feature fusion and further improve the performance of the network.

3.3 Improve the feature fusion module

In Yolov8n, the main role of the C2f (Channel-to-feature) module is to fuse feature maps of different scales. Through a feature fusion method called "concat", it concatenates the feature maps from different levels according to the dimension of the channel, and stacks them into a deeper feature map. This can retain more spatial information and semantic information, which is crucial for the performance improvement of object detection. In simple terms, C2f uses a variant of the Bottleneck module in the network structure to achieve feature fusion by serially connecting multiple Bottleneck modules and fusing them with the output of the last Bottleneck.

This design aims to improve the learning ability and efficiency of the network, but at the same time, because each Bottleneck module contains a convolution operation, the computational load and complexity of the whole C2f module increase. Although this structure can learn rich feature representations, it may face the problem of excessive consumption of computing resources in practical applications.

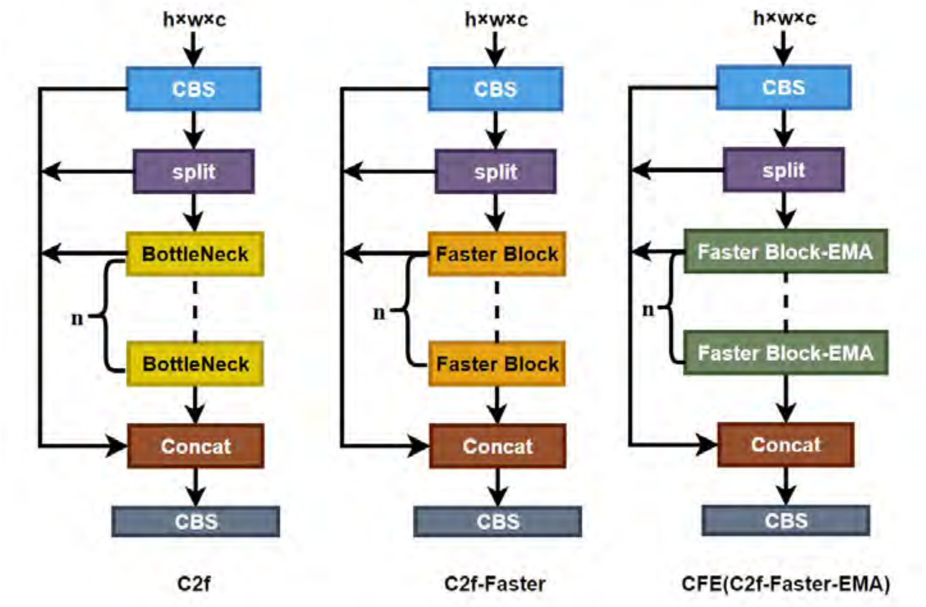

Fig. 3. Structure diagrams of C2f, C2F-Faster, and CFE

Therefore, in order to further reduce the size of the model and improve the computational efficiency, a lightweight C2f-Faster module is designed in this paper, and its structure is shown in Figure 3. The Bottleneck module in C2f is replaced by the FasterNet Block in FasterNet[21], which achieves an effective reduction in model size. EMA effectively solves the shortcomings of the traditional attention mechanism and shows excellent computational efficiency and generalization ability. By exploiting the flexibility and lightweight features of EMA, we integrate it into the C2f-FasterNet block, resulting in (CFE) C2F-FasterNet-EMA, as shown in Figure 3.

The CFE module significantly improves the perception ability of the model. The core of this improvement is that it combines multi-scale feature fusion technology and complex attention mechanism, which enables the model to finely capture and fuse the context information and multi- dimensional features from different scales of objects, thus making its perception of objects more acute and comprehensive.

3.4 Improving the neck structure

In the Yolov8n algorithm model, the neck network is the part that connects the backbone network and the head network of the convolutional neural network (CNN), which is responsible for feature fusion and processing, so as to improve the accuracy and efficiency of detection. Slim- neck is a design paradigm designed to optimize the neck network part of a convolutional neural network.

In order to solve the speed problem of convolutional neural network prediction calculation, Li[15] et al. proposed a design paradigm based on GSConv, namely Slim-Neck. The main feature is to use lightweight convolution module GSConv instead of traditional SC convolution to improve the representation ability of the model and reduce the computational cost. The specific implementation is shown in FIG. 4. Firstly, an ordinary down-sampling convolution is performed on the input feature map, and then it is concatenated with the feature map after deep convolution. The channels corresponding to the first two convolutions are concatenated by Shufe operation to fully fuse the information obtained by SC convolution and DSC convolution.

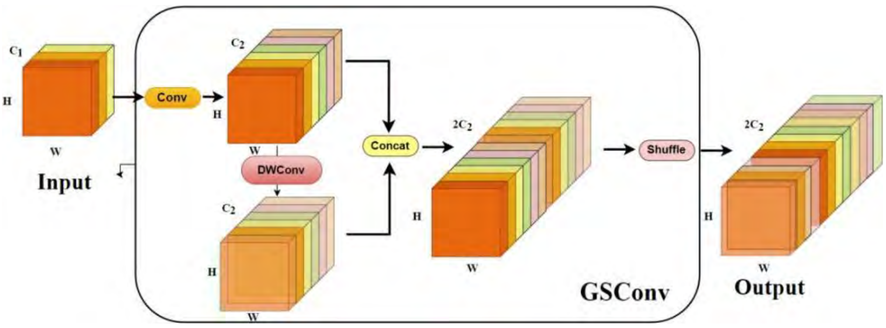

Fig. 4. GSConv structure diagram

In the PCB surface defect detection model, the one-time aggregation method is used to design the cross-stage Partial Network (GSCSP) module VoV-GSCSP. The VoV-GSCSP module reduces the complexity of calculation and network structure, but maintains sufficient accuracy. Figure 5 shows the structure of VoV-GSCSP.

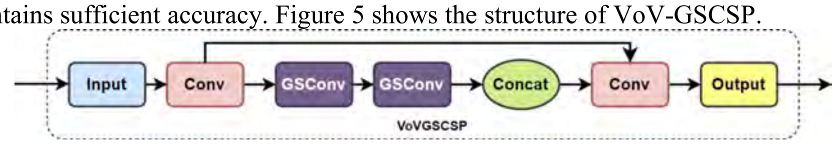

Fig. 5. Structure diagram of VoV-GSCSP module

Firstly, through the design of one-time aggregation method, VoVGSCSP can effectively fuse information between feature maps at different stages, thereby significantly improving the ability of the model to extract PCB surface defect features. This feature is crucial for capturing subtle defects and helps to improve the accuracy of detection. Secondly, considering that PCB surface defect detection needs to process a large amount of image data, which has certain requirements for computing resources, the VoVGSCSP module realizes the lightweight design of the model while ensuring the detection accuracy, reduces the computational complexity and reasoning time, and is more suitable for deployment in the actual production environment. In addition, there are many kinds of PCBS, and the surface defects are also different. Through its efficient feature fusion mechanism, VoVGSCSP module helps to enhance the generalization ability of the model to different types of PCB surface defects and improve the robustness of detection. In summary, the VoVGSCSP module not only improves the accuracy of PCB surface defect detection, but also accelerates the detection speed, makes the model more adaptive to the complex background environment, and reduces the overall deployment cost, which has significant advantages in PCB surface defect detection tasks.

4 Experimental results and analysis

4.1 *Experimental environment and evaluation index*

The experimental platform is based on 64-bit Windows 10 operating system, the CPU is 11th Gen Intel(R) Core(TM) i7-11800H @ 2.30GHz, the GPU is NVIDIA GeForce RTX 3060, and the memory is 32GB. The language used in the experiment was Python 3.9.16, and the deep learning framework version was PyTorch 2.0.1+ CUDA 11.7.

Table 1. Experimental parameters

Experimental parameters	Parameter quantity
Epoch	100
Patience	50
Optimizer	auto
Batch	8
Image Size	640
Learning rate	0.01

Several core metrics play a crucial role when evaluating the performance of a network model.The first is Precision (P), which measures the fraction of samples predicted by the model as positive that are actually positive. Next is Average Precision (AP), which calculates the accuracy for each class and averages it to give a comprehensive picture of the model's performance on different classes. Another important metric to evaluate is Recall (R), which is the fraction of samples that were actually positive that were correctly predicted as positive by the model. In particular, mean Average Precision (mAP) is the average of AP values of multiple classes, which can more comprehensively evaluate the overall performance of the model. In this paper, mAP@0.5 is selected as the specific evaluation index, which means that the Intersection Over Union (IoU) threshold of 50% is used in the calculation of mAP. The higher the mAP@0.5 value, the better the overall performance of the model in the detection task.

In addition to the above performance evaluation metrics, two important Parameters, Parameters and FPS, are introduced to consider the lightweight degree of the model. The total number of model Parameters reflects the number of parameters that need to be optimized during the training process of the model, which is an important indicator to evaluate the complexity and computational requirements of the model. FPS (Frames Per Second) is directly related to the detection speed of the model, indicating the number of images that the model can process per second or the time it takes to process a single image. The higher the FPS value, the faster the detection speed of the model, and the more suitable for real-time applications. In summary, through the three key indicators mAP@0.5, Parameters and FPS, we can comprehensively and accurately evaluate the comprehensive performance of the network model in terms of performance and lightweighting.

4.2 *Experimental* Data

The dataset used in this experiment is the open source PCB surface defect dataset PKU- Market-PCB released by the Open Laboratory of Intelligent Robotics of Peking University in 2019. The dataset contains a total of 693 images, covering six common defect types: excess copper, missing solder joint, burr, open circuit, short circuit, and gap. In order to simulate different image shooting angles and the random occlusion that may occur when PCB defects exist, the experiment uses a variety of methods for data enhancement processing, such as mirror flipping, adding noise, and randomly resizing cropping. Considering that in engineering applications, there may be various complex situations when using industrial cameras for image acquisition, these data enhancement methods are of great significance to improve the generalization ability and practical application effect of the model. The expanded data set consists of 6408 images. As shown in Table 2, the training set and test set are divided according to 8:2, respectively.

Table 2. Data set Detail type Table

Type	train	valid	Total
spurious_copper	603	149	752
spur	583	145	728
mouse_bite	619	142	761
missing_hole	635	140	775
short	614	146	760
open_circuit	617	147	764
RandomResizedCrop	543	74	617
Blur	559	63	622
SafeRotate	552	77	629
Total	5325	1082	6408

4.3 Ablation experiments

In order to verify the practical effects of the improved measures proposed in this paper, a set of ablation experiments were designed for in-depth comparison and analysis. To ensure the fairness and accuracy of the experimental results, all experiments were performed under the same parameter Settings, and the expanded data set was used as the test benchmark. The specific results of ablation experiments are summarized in Table 2, where the "√" symbol represents that the corresponding module is adopted in the experiment, and the "×" symbol indicates that the module is excluded from the experiment. Through this detailed set of ablation experiments, we can clearly evaluate the specific contribution of each improvement to the overall performance.

Table 3. Analysis of improved experimental results

Model		**Yolov8n**	**F-Yolov8n**	**FE-Yolov8n**	**FEV-Yolov8n**
C2f-Faster		x	√	√	√
C2f-Faster-EMA		x	x	√	√
VoVGSCSP		x	x	x	√
AP/%	spurious_copper	83.99	81.23	82.23	86.63
	spur	85.84	81.17	85.17	87.00
	mouse_bite	94.31	93.35	93.35	93.60
	missing_hole	99.11	99.16	99.16	99.42
	short	96.68	94.83	94.83	95.91
	open_circuit	92.43	92.58	92.58	92.67
mAP@ 0.5/%		92.06	90.38	91.22	92.54
FPS		212.77	204.08	187.35	175.44
Parameters /M		3.157	2.796	2.800	2.681

Among them, YOLOv8n is used as the starting baseline model, and its performance forms the basis for subsequent improvements. In order to further improve the performance of the model, F-YOLOv8n is first introduced. This version replaces the original Bottleneck structure of the key C2f module in Backbone with a more efficient FasterNet Block through fine architecture adjustment, which aims to enhance the feature extraction ability of the model. At the same time, it may bring about an improvement in computational efficiency. Then, FE-YOLOv8n goes a step further by not only maintaining the advantages of FasterNet Block, but also comprehensively upgrading the C2f module to a customized CFE lightweight feature extraction module, which significantly reduces the computational burden of the model and ensures the quality of feature extraction, making the model more lightweight while maintaining performance. Finally, as the integrator of this series of improvements, FEV-YOLOv8n not only optimizations at the Backbone level, but also delves into the

Neck part of the model. By introducing the ingenious combination of VoVGSCSP structure and Slim neck design, the ability of the model to deal with complex features is further improved. At the same time, it maintains efficient detection speed, which provides a more powerful and flexible solution for practical application scenarios.

Table 3 shows that the Parameters of F-Yolov8n, FE-Yolov8n and FEV-Yolov8n are lower than those of the baseline Yolov8n model, and these improved models reduce the Parameters of PCB defect detection by 0.12%, 0.11% and 0.15%, respectively. The lightweight effect of PCB defect detection model is improved. For F-Yolov8n, using the Faster lightweight feature extraction module can greatly compress the number of parameters of the model, but with the rapid reduction of the model accuracy. After the introduction of the CFE module, compared with the baseline model, the total number of parameters and FPS value are reduced to a certain extent, and the lightweight effect of the model is further improved. Because the lightweight module introduces efficient multi-scale attention EMA, the model is able to capture deeper semantic information. mAP@0.5 is 0.84% higher than the F-Yolov8n model, which also proves the feasibility of CF- EMA in improving the performance of the model. Using VoVGSCSP combined with Slim-neck structure for optimization in the neck, although the accuracy of the model is slightly increased compared with the baseline model Yolov8n, the number of parameters is greatly reduced, and the mAP@0.5 value is increased to 92.54%. Among them, the detection accuracy of the difficult to distinguish spurious_copper and spur defect categories was most significantly improved, increasing by 2.64% and 1.16%, respectively.

4.4 Comparative experiment

The current mainstream algorithms for object detection include SSD, Faster R-CNN, YOLOv5, YOLOv7, etc. After training this dataset with these mainstream algorithms, the verification results obtained are compared with the results of the improved model in this paper. The mAP value is used as the model evaluation index, and the experimental results are shown in Table 3.

Table 4 Analysis of comparative experimental results

Algorithm	mAP (%)	FPS	Parameters /M
SSD	89.28	72.519	6.864
Faster R-CNN	91.93	35.13	11.527
Yolov5	90.67	178.59	2.386
Yolov7	87.35	156.51	8.516
Yolov8	92.06	212.77	3.157
FEV-Yolov8n	92.54	175.44	2.681

According to the data in Table 4, it can be seen that the FEV-Yolov8n algorithm proposed in this paper has a significant improvement in detection performance compared with SSD, Faster R- CNN and Yolov7 algorithms. In terms of detection accuracy, the FEV-Yolov8n algorithm is 3.26%, 0.61%, and 5.19% higher than other algorithms mAP@0.5. In terms of parameter scale, the FEV- Yolov8n algorithm decreased by 60.9%, 76.7% and 68.5% compared with other algorithms, respectively. This shows that the FEV-Yolov8n algorithm proposed in this paper reduces the complexity of the model while maintaining high accuracy. Although compared with Yolov5, the parameter size of the proposed algorithm is slightly increased, the key indicator mAP@0.5 is increased by 1.87 percentage points, showing its performance advantage in PCB defect detection. In terms of video detection speed, the improved FEV-Yolov8n is lower than that of Yolov5 and Yolov8, but its advantage is still significant compared with other algorithms such as SSD and Faster R-CNN. Compared with the original network Yolov8n, the optimized FEV-Yolov8n algorithm has an improvement of 1.8%in the mAP@0.5 index, which proves its effectiveness in improving the detection accuracy.

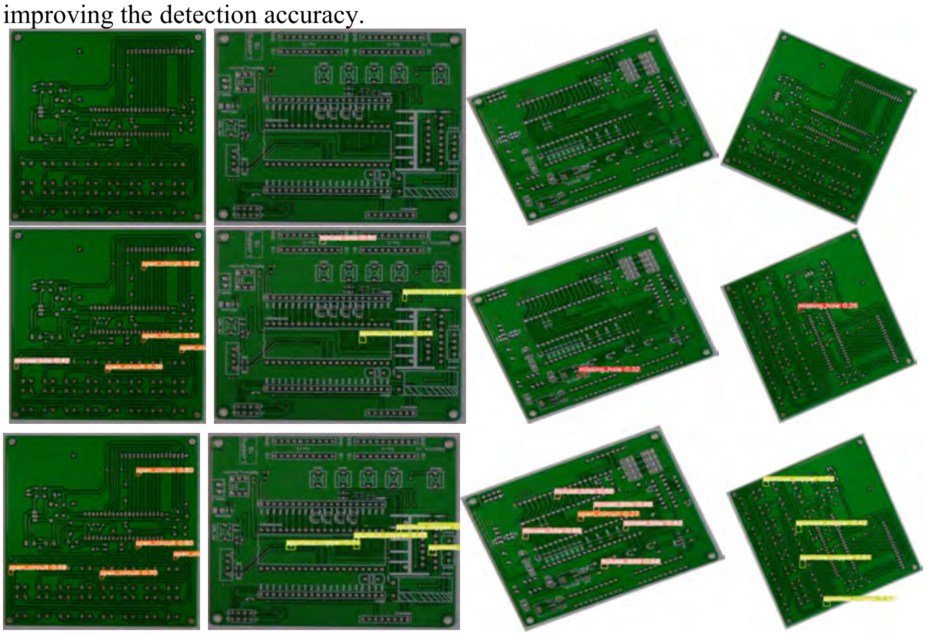

Fig. 6. Comparison of the PCB defect detection effect

(From top to bottom are Original Image\Yolov8n\FEV-Yolov8n)

In order to verify the actual detection effect of the FEV-Yolov8n algorithm under different quality images, we selected the representative PCB defect images in the data set that were difficult to detect for verification. The detection effect is shown in FIG. 6. Under the poor image quality with noise and low light background, the original Yolov8n algorithm has obvious missed detection and false detection phenomenon, especially the two defects of spurious_copper and spur that are difficult to distinguish. Secondly, when the Angle changes, the detection effect of the original Yolov8n algorithm model decreases sharply. On the contrary, the FEV-Yolov8n algorithm can deal with this situation well, and has good robustness and anti-interference.

5 Conclusion

Taking Yolov8n as the benchmark model, this paper proposes a lightweight defect detection model FEV-Yolov8n for PCB. The purpose is to improve the accuracy of the existing model algorithm for PCB defect detection while balancing the detection efficiency. Firstly, the FasterBlock module is introduced into the C2f module in the backbone network to form a lightweight feature extraction module C2F-Faster, which greatly reduces the number of parameters of the model. Then, the cross-spatial multi-scale attention mechanism is integrated into the improved C2f-Faster module. By automatically adjusting the attention weight according to the current input context, the model can pay more attention to important information while ignoring irrelevant information, so as to improve the accuracy decline caused by the improvement of detection rate. Finally, the neck network structure is designed, and the Slim-neck neck structure based on the VoVGSCSP module is constructed. The one-time aggregation method is used to design, which can effectively fuse information between the feature maps of different stages, so as to improve the model's ability to detect the target, and reduce the complexity of calculation and network structure while maintaining sufficient accuracy. This lightweight design enables the model to process images faster in the inference process and reduces the consumption of computing resources.

The ablation and comparison experiments demonstrate that the introduction of FasterBlock module reduces the computational complexity and memory occupation of the model, improves the reasoning speed of the model, and the number of parameters of the original model is reduced by 0.12%. The secondary combination of CMA attention mechanism helps C2f module to extract and identify key features more accurately. The dynamic weight adjustment ability of EMA enables the model to focus more on the features that are crucial to the detection task, so as to improve the detection accuracy and balance the accuracy. The parameter amount is reduced by 0.11%, and mAP@0.5 is 0.84% higher than that of F-Yolov8n model. Finally, the Slim-neck neck structure based on the VoVGSCSP module is improved, so that the model can complete the detection task faster while maintaining high accuracy. The improved FEV-Yolov8n model has the parameter amount reduced by 0.15%, and the accuracy also reaches 92.54%.

However, there are still some shortcomings in this study. The data set used is only the surface data set of PCB bare board, and the situation on the circuit board such as more complex components and wiring is not considered. In the future, the study of complex background and small target defects can be further carried out after collecting and labeling or obtaining open- source authoritative data sets.

References

1. Lu Rongsheng, WU Ang, Zhang Tengda, et al. Acta Optica Sinica,2018,38(08):23-58. (in Chinese with English abstract)
2. REN S,HE K,GIRSHlCK R,et al.Faster R-CNN:towards real-time object detection with region proposal networks[Jl.lEEE Transactions on Pattern Analysis and Machine Intelligence,2017.39(6):1137-1149.
3. REDMON J, DIVVALA S, GIRSHICK R, et al. You only look once: Unified, real- time object detection[C]// Proceedings of the IE conference on computer vision and pattern recognition. 2016: 779-788.
4. REDMON J, FARHADI A. YOLO9000: better, faster, stronger[C]//Proceedings of the IEEE conference on computer vision and pattern recognition. Honolulu: EEE, 2017: 7263-7271.
5. REDMON J, FARHADI A. Yolov3: An incremental improvement[C]//Computer vision and pattern recognition. Berlin/Heidelberg, Germany: Springer, 2018: 1-6.
6. Hu Lanlan, Deng Chao. PCB defect detection algorithm Based on YOLO-MCG [J]. Instrument Technology and Sensor,2024(04):100-106.
7. Xu Haoxiang, Shu Guohua. PCB Defect Detection Algorithm Based on Lightweight YOLOv5 [J]. Electrical Automation,2024,46(02):95-97+102.
8. Li Zhongke, Liu Xiaofang. PCB defects detection algorithm based on lightweight YOLOv8n networks [J]. Journal of electronic measurement technology, 2024,47 (4) : 120-126. The DOI: 10.19651 / j.carol carroll nki emt. 2315076.
9. LIAO Xinting, ZHANG Jie, LV Shengping. Fusion of shallow characteristics and attention mechanism PCB defect detection method [J]. Journal of computer integrated manufacturing system, 2024, 30 (03) : 1092-1104. The DOI: 10.13196 / j.carol carroll ims.2023.0039.
10. Fang Qiang. Bare PCB board surface defect detection based on deep learning algorithms [D]. Nanchang engineering institute, 2023. The DOI: 10.27839 /, dc nki. GNCGC. 2023.000042.
11. Li X C. PCB Polar Component defect Detection based on Improved Faster RCNN [D]. Chongqing university of posts and telecommunications, 2022. DOI: 10.27675 /, dc nki. Gcydx. 2022.000406.
12. Dong X J. Research and implementation of rapid detection system of PCB board defects on mobile terminal based on lightweight Convolutional Neural Network [D]. Yangtze university, 2023. DOI: 10.26981 /, dc nki. GJHSC. 2022.000287.
13. CHEN J,KA0 S,HE H,et al.Run,don't walk:chasing higher FLOPS for faster neural networks[C]//Proceedings of the lEEE/CVF Conference on Computer Vision and Pattern Recognition,2023:12021-12031.
14. OUYANG D, HE S, ZHANG G, et al. Efficient Multi-Scale Attention Module with Cross-Spatial Learning[C]//ICASSP 2023-2023 lEEE International Conference on Acoustics, Speech and Signal Processing (lCASSP).IEEE,2023:1-5.
15. LI H L,Ll J,WEl H B,et al. Slim-neck by GSConv:a better design paradigm of detector architectures for autonomous Vehicles [EB/ 0 l]. 2022:arXiv:2206.02424.http:/larxiv.org/abs/2206.02424.